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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,225	07/02/2003	Chih-Chin Chang	ADTP0054USA	1224

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,225	CHANG, CHIH-CHIN	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/7/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *18-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species I claims 1 – 17 in Paper No. filed May 7, 2004 is acknowledged. The traversal is on the ground(s) that the two species disclose a method of forming a self-aligned LTPS TFT utilizing the gate conductive layer in forming the source and drain and the LDD in a self-aligned way. This is not found persuasive because although the species achieve the same goal, they achieve the goal by two different embodiments (different method steps), which constitute two separate inventions. Searching for the two inventions at the same time will place additional burden on the examiner.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 18 – 30 were withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Species II claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. filed May 7, 2004.

Specification

3. The disclosure is objected to because of the following informalities: In paragraph 26, last line 14, the word "NLTPS" should be changed to "PLTPS".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 2 and 6 – 9 and 12 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ayres, US 6,632,709.

Regarding claim 1, The APA teaches a method of forming self-aligned LTPS TFT comprising the steps of:

- providing a substrate 10 comprising an N type LTPS TFT region I and a P type LTPS TFT region II as shown in Fig. 1;
- sequentially forming a patterned undoped polysilicon layer 12, a dielectric layer 14, and a patterned conductive layer 16, the patterned conductive layer comprising two first gaps on both sides of layer 16 (see Fig. 1);
- performing a first implantation process 38 to implant N type dopants 18 via the first gaps into the undoped patterned polysilicon layer 12 to form a source and a drain 20 as shown in Fig. 2;

- performing a second implantation process to implant N type dopants into the undoped patterned polysilicon layer 12 to form two lightly doped drains 26 (see Fig. 3),
- forming a gate 16 of a P type LTPS TFT in the P type LTPS TFT region II, and forming a source and a drain 32 of the P type LTPS TFT in the P type LTPS TFT region II with reference to Fig. 4 as described in APA in paragraphs 7 – 9.

The APA fails to teach the steps: removing a certain width of the patterned conductive layer to form two second gaps and to define a gate of an N type LTPS TFT; and performing a second implantation process to implant N type dopants via the second gaps into the undoped patterned polysilicon layer to form two lightly doped drains.

Ayres teaches a method of forming self-aligned TFT in which he teaches removing (etching back) a certain width of the patterned conductive layer (gate layer) to form two second gaps and to define a gate of the TFT in column 1, line 56; and performing a second implantation process to implant N type dopants via the second gaps into the undoped patterned polysilicon layer to form two lightly doped drains in column 2, lines 38 – 42 for the benefit of operating the TFTs at relatively low biases and to reduce the series resistance of the region in column 2, lines 42 – 49.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the APA and form the TFT by removing a certain width of the patterned conductive layer to form two second gaps and to define a gate of an N type LTPS TFT; and performing the second implantation process to implant N type dopants via the second gaps into the undoped patterned polysilicon layer to form two

lightly doped drains for the benefit of operating the TFTs at relatively low biases and to reduce the series resistance of the region as taught by Ayres in column 2, lines 42 – 49.

Regarding claim 2, the APA teaches glass substrate in paragraph 6.

Regarding claim 6, the APA teaches forming a first conductive layer and a first patterned photo resist layer on the dielectric layer, removing the conductive layer that is not covered by the first patterned photo resist layer to form the two first gaps in the conductive layer of the N type LTPS TFT region and removing the reduced first patterned photo resist layer in paragraph 7, but fails to teach performing a trimming process to reduce a certain width of the first patterned photo resist, removing the conductive layer that is not covered by the reduced first patterned photo resist layer, such that the two second gaps are formed in the conductive layer of the N type LTPS TFT region.

Ayres teaches a method of forming self-aligned TFT in which he teaches removing (etching back) a certain width of the patterned conductive layer (gate layer) to form two second gaps and to define a gate of the TFT as was explained earlier in rejecting claim 1 for the benefit of operating the TFTs at relatively low biases and to reduce the series resistance of the region. Ayres does not teach performing a trimming process to reduce a certain width of the first patterned photo resist, removing the conductive layer that is not covered by the reduced first patterned photo resist layer.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Ayres and perform a trimming process to reduce a certain width of the first patterned photo resist, removing the conductive layer that is not

covered by the reduced first patterned photo resist layer, since the etching of the conductive layer can be more simply carried out by the simpler photo etching process as taught by the APA instead of the complex anodization process by Ayres.

Regarding claim 7, Ayres teaches that the second gap is larger than the first gap due to the etching of the gate layer (see Fig. 10).

Regarding claim 8, the APA teaches aluminum in paragraph 7.

Regarding claim 9, Ayres teaches plasma ashing for the resist in column 10, lines 25 – 26.

Regarding claims 12 – 15, the limitations of these claims are taught by the APA in paragraphs 9 – 12 with reference to Figs. 4 – 5.

Regarding claims 16 and 17, the APA teaches these limitations in paragraph 5.

7. Claims 3 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ayres, US 6,632,709 as applied to claim 1 above, and further in view of Yamazaki, US 5,210,050.

Regarding claim 3, the APA fails to teach the buffer layer between the substrate and the polysilicon layer.

Yamazaki teaches a TFT forming method in which he forms a silicon oxide film 12 buffer layer on the glass substrate 11 before forming the polysilicon layer 13 (see Fig. 1A) for the benefit of preventing interfacial reaction of the film with the glass substrate during crystallization of the film in column 4, lines 1 – 15.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the APA and form a buffer layer between the substrate

and the polysilicon layer for the benefit of preventing interfacial reaction of the film with the glass substrate during crystallization of the film as taught by Yamazaki in column 4, lines 1 – 1.

Regarding claim 4, the APA teaches forming an amorphous silicon (a-Si) on the substrate, performing an annealing process such that the amorphous silicon layer is recrystallized and turned a polysilicon layer, and performing a photo-etching process (PEP) to form a patterned undoped polysilicon layer in each polysilicon layer of the N type LTPS TFT region and the P type LTPS TFT region in paragraph 7, but fails to teach performing a sputtering process to form an amorphous silicon (a-Si) on the substrate.

Yamazaki teaches sputtering process to form an amorphous silicon (a-Si) film on the substrate for the benefit of producing a very low impurity film in column 3, lines 40 – 45.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the APA and form the form an amorphous silicon (a-Si) film on the substrate for the benefit of producing a very low impurity film as taught by Yamazaki in column 3, lines 40 – 45.

Regarding claim 5, Yamazaki teaches forming the dielectric layer comprising silicon oxide in column 5, lines 26 – 28.

8. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ayres, US 6,632,709 as applied to claim 1 above, and further in view of Liang, US 5,702,988.

Regarding these claims, APA in view of Ayres fails to teach the dopant concentration in the first implantation process is about 1E14 to 1E16 atoms/cm^2 and the N type dopants comprise arsenic or phosphorous and the dopant concentration in the second implantation process is about 1E12 to 1E14 atoms/cm^2 and the N type dopants comprise arsenic or phosphorous.

Liang teaches that source and drain and LDD regions can be formed by ion implantations as a standard procedure at dopant types and concentrations for the first implantation process at about 1E14 to 1E16 atoms/cm^2 and the N type dopants comprising arsenic or phosphorous and the dopant concentration for the second implantation process is about 1E12 to 1E14 atoms/cm^2 and the N type dopants comprising arsenic or phosphorous in between column 8, line 52 and column 9, line 15.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the APA in view of Ayres and form the source/drain and LDD regions at the dopant concentration for the first implantation process at about 1E14 to 1E16 atoms/cm^2 and the N type dopants comprising arsenic or phosphorous and the dopant concentration form the second implantation process at about 1E12 to 1E14 atoms/cm^2 and the N type dopants comprising arsenic or phosphorous as standard procedure as taught by Liang in between column 8, line 52 and column 9, line 15.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
May 26, 2004

Patent Examiner